

Remarks

Claims 1-30 are at issue. Claims 1-7 & 9-10 stand rejected under 35 USC 103(a) as being unpatentable over Barr et al (5,873,076). Claim 8 stands rejected under 35 USC 103(a) as being unpatentable over Barr et al (5,873,076) in view of Barrett et al (6,490,584). Claims 11 & 19 stand rejected under 35 USC 103(a) as being unpatentable over August et al (6,647,383). Claims 12-14 stand rejected under 35 USC 103(a) as being unpatentable over August et al (6,647,383) in view of Brown et al (6,665,666). Claims 15-18 & 20-30 stand rejected under 35 USC 103(a) as being unpatentable over August et al (6,647,383) in view of Barr et al (5,873,076).

The Examiner has complained that the specification does not include a Brief Summary of the Invention. There is no statutory or regulatory requirement that the specification include a Brief Summary of the Invention. The rejection must be withdrawn.

The Examiner has a number of 103 obviousness rejections, that only have a single reference. This amounts to an Official Notice rejection, and the applicants traverse these Official Notice rejections and demand that the Examiner find a reference to support their position.

Claim 1 requires an associative memory. The term associative memory is a very well defined term in the computer software field. See the attached definition from the *Computer Dictionary Online*. There is no discussion of associative memories or content addressable memories in Barr et al. Claim 1 is allowable.

Claim 2 requires a preparser. The specification defines a preparser 156 on page 15, lines 12-24. It makes it clear that the preparser is used to eliminate formatting characters that would interfere with the search. The section pointed to by the Examiner discusses parsing for natural language queries. Clearly this is not a preparser, it's a parser, and does not meet the definition in the specification. Claim 2 is allowable.

Claim 3 requires a hit output queue. The hit output queue is discussed on page 16, lines 6-12. The section pointed to by the Examiner discusses a queue for the searches not the hits. Claim 3 is allowable over the prior art.

Claims 4–6 & 9 are allowable as being dependent upon an allowable base claim.

Claim 7 requires a transform generator. The specification explains on page 6, lines 16 – 21 that the transform is a CRC or any linear feedback shift register transformation. The section pointed to by the Examiner does not perform a CRC or a linear feedback shift register transformation. Claim 7 is allowable over the prior art.

Claim 8 requires the data be converted into an address and a confirmer. The section pointed to by the Examiner only discusses an address, it does not discuss converting data into an address or a confirmer. Claim 8 is allowable over the prior art.

Claim 10 requires an input packet queue. The section pointed to by the Examiner does not discuss input packet queues. Claim 10 is allowable.

Claim 11 requires a sliding window search. A sliding window search is discussed on page 6, lines 5-10. The sliding window search is a way of matching data to a search term or terms. The section pointed to by the Examiner is just a filter for the time, it does not slide along the bytes of data. Claim 11 is allowable over the prior art.

Claim 12 requires parsing the raw data. The section pointed to by the Examiner is discussing the query data not the data to be searched. Claim 12 is allowable.

Claim 13 requires replacing the white characters in the raw data. This is not shown nor is it obvious in light of the prior art. Claim 13 is allowable.

Claim 14 is allowable for the same reasons as claim 12.

Claim 15 requires a proximity key list and a primary index. This is not shown in Barr or any of the prior art. Claim 15 is allowable.

Claim 16 requires a next list. This is not shown in August. Claim 16 is allowable.

Claim 17 is allowable for the same reasons as claim 16.

Claim 18 is allowable for the same reasons as claim 16.

Claim 19 requires removing overhead data from an input data stream. There is no discussion in August of an input data stream. Claim 19 is allowable.

Claim 20 requires an associate match memory. The term associative memory is a very well defined term in the computer software field. See the attached definition from the *Computer Dictionary Online*. There is no discussion of associative memories or content addressable memories in Barr et al. In addition, claim 20 requires a sliding search engine. A sliding window search is discussed on page 6, lines 5-10. The sliding window search is a way of matching data to a search term or terms. The section

pointed to by the Examiner is just a filter for the time, it does not slide along the bytes of data. Claim 20 is allowable over the prior art.

Claims 21 & 22 are allowable for the same reason as claim 20.

Claim 23 requires a preparser. The specification defines a preparser 156 on page 15, lines 12-24. It makes it clear that the preparser is used to eliminate formatting characters that would interfere with the search. The section pointed to by the Examiner discusses parsing for natural language queries. Clearly this is not a preparser, it's a parser, and does not meet the definition in the specification. Claim 23 is allowable.

Claim 24 requires a mapping table. The Examiner's Official Notice is traversed.

Claim 25 is allowable for the same reason as claim 24.

Claim 26 is allowable for the same reasons as claim 20.

Claims 27 & 29-30 are allowable as being dependent upon an allowable base claim.

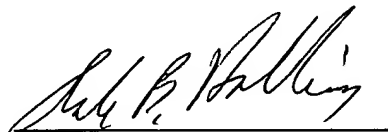
Claim 28 requires a primary index and a next index. This is not shown in the prior art. Claim 28 is allowable.

The application has been placed in condition for allowance, prompt reconsideration and allowance are respectfully requested.

Respectfully submitted,

(Brandin)

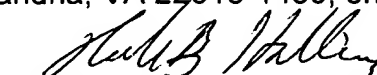
By



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content addressable memory

[a](#) [b](#) [c](#) [d](#) [e](#) [f](#) [g](#) [h](#) [i](#) [j](#) [k](#) [l](#) [m](#) [n](#) [o](#) [p](#) [q](#) [r](#) [s](#) [t](#) [u](#) [v](#) [w](#) [x](#) [y](#) [z](#)

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content addressable memory

(CAM, or "associative memory") A kind of storage device which includes comparison logic with each bit of storage. A data value is broadcast to all words of storage and compared with the values there. Words which match are flagged in some way. Subsequent operations can then work on flagged words, e.g. read them out one at a time or write to certain bit positions in all of them. A CAM can thus operate as a data parallel (SIMD) processor.

CAMs are often used in caches and memory management units.

(1995-02-16)

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